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A Fault Synchronized Impedance Measurement Design for Digital Distance Protection

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Abstract: *This paper presents an algorithm for microprocessor based design, developed around Intel 8086 to measure the transmission line impedance with fault synchronized sampling data of line voltage and current signals for digital distance protection. The value of impedance from relay location to fault point is required to be known in order to determine whether the fault point occurs in the protective zone of relay or not. Usually data sampled at a pre-specified rate are used by an algorithm to measure the fault impedance which are compared with relay setting for making decision. The measurement of fault impedance with non fault synchronized sampling frequency is not accurate from comparing point of view to locate fault point because the values of di/dt are different for different values of phase angle.*

Keywords: *MODEL Transmission Line, Shunt Capacitance, Transient High Frequency Components, Differential Equation Solution, Digital Distance Relays.*

1. INTRODUCTION

A fast fault clearing reduces the risk of power system transient instability and thermal stress on connected equipments. Hence to improve transient stability of the complex power system, it is required to keep the fault clearing time as short as possible. Therefore in order to get better performance of protective scheme of transmission line with connected equipments in complex power system, more fast, accurate and computationally simple algorithm is needed. In general data sampling rate used by the algorithms are same for both pre-fault and post-fault conditions i.e. non-fault synchronized. In fact under fault conditions, the transient frequency varies with nature of faults and distance of fault from the relay location. Hence the same sampling frequency in both conditions can not be able to sample the signal at the same phase angle that may cause to measure incorrect impedance from comparing point of view to locate the fault point, because the values of di/dt are different for different values of phase angle. The proposed fault synchronized algorithm is auto fast and accurate than that of non fault synchronized algorithm which can achieve improved performance and also easily fulfill the present requirements of modern protective relays.

A number of algorithms were reported for digital distance relaying [1-14] during last three decades; the algorithm based on differential equation representing the transmission line model by series impedance circuit is the fastest and most suitable algorithm in implementing the protective relaying based on microprocessor [3-8]. The differential equation solution based on series impedance transmission line model does not include any line shunt capacitance. As a result, the relay will calculate incorrect line impedance in presence of high frequency transient components. Clearly, algorithm is not accurate. Hence, system stability is affected. Therefore, to improve the stability of the system particularly for medium and long transmission line, it is necessary to consider the shunt capacitance of transmission line for more accurate protective relaying design. Hence, in the present scheme, a π-model transmission line is considered instead of R-L model [8-11].

Since the shunt capacitance is not included in differential equation solution based on series R-L model transmission line, hence in presence of high frequency transient components under fault conditions, this algorithm cannot be used to calculate the line impedance particularly for EHV/UHV transmission line without the addition of low pass filter to remove any such high frequency transient that have not been removed by the algorithm itself. The proposed algorithm used for design is based on differential equation solution using π-model transmission line, which accommodates transient high frequency components of line voltage and current signals without any additional filtering of these transients. In this design, sampling frequency of voltage and current signals synchronize automatically with high transient frequency without any change in interface or software design.

With the advancement in VLSI technology more economical, powerful and sophisticated microprocessors are available today. So, its applications to complex power

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system are the current interest for the power protection engineers. The main attraction to design and develop the microprocessor-based systems for power system protection is its economy, compactness, reliability and flexibility due to programmability. The aim of this paper is to present design, and development of microprocessor based system for measurement of transmission line fault impedance for digital protective relay with fault synchronized signal sampling. The algorithm used is based on the solution of differential equation representing π-model transmission line. It is the fastest and most simple and suitable for microprocessor implementation of distance relays. In the proposed design fault impedance measurement frequency simultaneously synchronizes with high transient frequency. Hence, this technique is as fast as high frequency transient and accurate.

2. ANALYSIS OF FAULTED π-MODEL TRANSMISSION LINE

In Figure (1a), a single phase equivalent π-model transmission line having series resistance R, series inductance L and shunt capacitance at each end C/2 is shown .Under post fault conditions ,a distance relay at sending end and a fault on the far end of line is shown in Figure 1(b). The fault resistance is assumed to be sufficiently small so that the far end line capacitance may be neglected.

Post fault π-model transmission line network can be characterized by the following differential equations:

At sending end,

$$v_S = Ri_L + L(di_L / dt) \tag{1}$$

$$i_s = i_{cs} + i_L$$

$$i_s = C/2\ (dv_S / dt) + v_S / Z_L \tag{2}$$

Equations (1) and (2) hold for both steady state and transient conditions. The occurrence of fault represents the transient conditions. Therefore, the value of transmission line parameters (R&X) under fault conditions are required to be known for distance relaying in order to determine whether the fault point lies in the protective zone or not.

3. ALGORITHM FOR IMPEDANCE

The solution for R &L from differential equation (1) can be obtained taking boundary conditions under consideration.

When $$i_L = 0,\ L = (v_S / di_L / dt) \tag{3}$$

and $$X_L = 2\pi f_L \tag{4}$$

When $$(di_L / dt) = 0,\ R = (v_S\ / i_L) \tag{5}$$

Further, C can be evaluated under boundary condition from equation (2)

When $$v_S = 0,\ C = 2\ (i_s / dv_S / dt) \tag{6}$$

$$X_C = 1 / 2\pi fc \tag{7}$$

The equations (3) to (7) are programmed to calculate the value of line parameters (R, X_L, X_C). The resistance R is the ratio of voltage to current at the instant when (di_L / dt) is zero. Inductance is the ratio of voltage to (di_L / dt) at the instant when current is zero. Shunt capacitance is the ratio of current to (dv_s / dt) at the instant when voltage is zero. Using the value of equation (4), (5) & (7) μP calculates fault impedance of transmission line.

4. MICROPROCESSOR BASED DESIGN

To implement the above algorithm for the measurement of transmission line parameters under fault or transient conditions, a prototype of Intel 8086 microprocessor based system has been designed, developed and successfully tested in the laboratory. The hardware and software design of the proposed microprocessor based system are described as below.

4.1. Hardware Design

Schematic block diagram of the microprocessor–based system is shown in Figure 2, the voltage and current signals are stepped down to electronic range using potential and current transformers. The current signal derived from the current transformer is converted into proportional voltage signal by using current to voltage converter. The data acquisition system (DAS) consists of active low pass filter, differentiator, and inverter, bipolar to unipolar converter, sample & hold circuit and multiplexer-cum-A/D converter (0809).

In laboratory the test, an active low pass anti aliasing filter is used in this design to attenuate a significant part of noise in signal for improved result and hence sampling frequency here depends upon cut-off frequency of low pass filter. The data acquisition system is interfaced to the microprocessor through Intel 8255 programmable peripheral interface. The voltage signal, current signal and differentiator output signal are connected to three input port of the 8255 through zero-cross detectors to examine whether these signals have crossed their zero point?

4.2. Software Design

The microprocessor reads the output of zero-cross detector connected to the current signal to examine whether the current has crossed its zero point or not. At the instant of zero current microprocessor reads the value of v_S and (di_L / dt) and calculate the value of inductive reactance X_L by using equation (4) Afterwards microprocessor reads the output of the zero-cross detector connected to the current differentiator output to examine whether (di_L / dt) has crossed its zero point. At the instant of (di_L / dt) microprocessor reads the value of zero-cross detector connected to the voltage signal to examine whether voltage has crossed its zero point. At the instant of voltage to be zero, microprocessor reads the value of *iS* and (dv_S / dt) and calculate the value of X_C by using equation (6) & (7).

Using calculated value of R, X_L & X_C any desired distance relay characteristic can be realized. The program flow chart is showing in Figure 3, for the measurement of transmission line parameters (R, X_L & X_C). A program in assembly language of the 8086 has been developed for the purpose.

In the π-model of transmission line variable R, L & C were set to represent different fault points. By using proposed algorithm the values of R, X_L & X_c were measured for different settings of R, L & C of the transmission line model. A prototype of Intel–8086 microprocessor based system has been designed, fabricated and tested in the laboratory.

5. CONCLUSIONS

Microprocessor reads every cycle of signal as it crossed zero point hence sampling frequency is automatically synchronized with fault high transient frequency. As a result impedance calculation is as fast as transient frequency and more accurate to that of non fault-synchronized sampling frequency. Any desired distance relay's characteristics can be realized with the measured value of transmission line parameters (R, L & C) by using the same interface circuit and changing the program only. The proposed scheme is also versatile and hence can be used for measurement of power system quantities and over current relaying too. Computational requirements of fault impedance calculation in the proposed algorithm are very simplified. It is accurate and very fast, hence suitable for microprocessor implementation of digital distance protection.

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